Roll No. | | | | | | | | | | | | **Total No. of Pages: 02**

Total No. of Questions: 09

MCA (2015 Batch) (Sem. – 6)

ADVANCED COMPUTER ARCHITECTURE

M Code: 74757

Subject Code: MCA-603

Paper ID: [74757]

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **Section A, B, C & D contains TWO questions each, carrying TEN marks each and students have to attempt at least ONE question from EACH SECTION.**
2. **Section E is COMPULSORY consisting of TEN questions carrying TWO marks each.**

SECTION A

1. a) What are the differences between hardwired and micro-programmed processors?

   b) How multi-core processor differs from pipeline processor? Explain.

2. What are the ways available to measure performance of pipeline processor? Explain.

SECTION B

3. How direct mapped cache differs from associative cache? Explain.

4. a) Explain how cache performance is measured and how it can be improved?

   b) Reducing hit time in a cache speedup the memory module. Comment.

SECTION C

5. Explain the following:

   a) Out of order execution

   b) Memory Disambiguation

6. What is meant by speculative execution? How branch prediction helps in improving the performance of pipeline processor? Explain.

SECTION D

7. Discuss the vital issues associated in designing a memory hierarchical module. 10

8. Explain the following:

   a) Memory protection 5

   b) Memory Synchronization 5

SECTION E

9. a) Compare Little Endian and Big Endian notations.

   b) What is Flynn's taxonomy?

   c) How data hazards can be minimized?

   d) State Loop Unrolling concept.

   e) What is an array processor?

   f) Define Snooping.

   g) Explain briefly WAW hazard.

   h) What is cycle by cycle interleaving?

   i) What is throughput?

   j) What are two key limitations of ILP?