**Roll No.** | | | | | | | | | | | | | **Total No. of Pages : 02**

**Total No. of Questions : 07**

**BCA (Sem–2)**

# COMPUTER SYSTEM ARCHITECTURE

**Subject Code : UGCA-1908**

**M.Code : 77416**

**Date of Examination : 02-06-2023**

**Time : 3 Hrs.** **Max. Marks : 60**

**INSTRUCTIONS TO CANDIDATES :**

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains SIX questions carrying TEN marks each and students have to attempt any FOUR questions.**

## SECTION-A

**1. Answer very briefly :**

a) Define a NOT and NAND gate using diagram.

b) What is a K-Map and write its use in boolean algebra.

c) Mention any two benefits of demultiplexer.

d) Show a parallel binary adder using a circuit diagram.

e) What is encoding and decoding?

f) How can we remove a race around condition?

g) Mention the features of RISC architecture.

h) Name the types of buses used in computer system architecture.

i) Why is D-Flip flop used?

j) What is the need of a register in computer system architecture?

## SECTION-B

2. Explain the Logic Gates : XOR, XNOR, NAND and NOR with neat diagram for each.

3. Compare the execution of half adder/subtractor with a full-adder/subtractor.

4. Simplify the expression using K-maps : F(A,B,C) = $\sum(1,3,5,6,7)$.

5. Show the logic diagram and explain J-K flip-flop and R-S flip-flop.

6. Explain in detail the Von Neumann architecture.

7. Describe the data movement among registers using bus in a 16-bit common bus system.

**NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student**.