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Total No. of Pages : 02

Total No. of Questions : 09

B.Tech. (AI&ML/AI&DS/CSE/ Block Chain/CS/DS/IOT/CSD/IT/ Robotics & Artificial Intelligence) / (Internet of Things and Cyber Security including Block Chain Technology) (Sem.-3)

DIGITAL ELECTRONICS

Subject Code : BTES301-18

M.Code : 76435

Date of Examination : 13-12-2025

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY** consisting of TEN questions carrying TWO marks each.
2. **SECTION-B** contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.
3. **SECTION-C** contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.

SECTION-A

1. **Write briefly:**

- a) Discuss the need of hexadecimal number system.
- b) Convert 1101110 to binary number to Gray code.
- c) What do you mean by combinational circuits? Explain.
- d) Discuss the significance of multiplexer.
- e) List the limitations of asynchronous counters.
- f) State DeMorgan's theorems.
- g) Differentiate between PROM and EEPROM.
- h) List the advantages offered by complex Programmable logic devices.
- i) Write down the various characteristics of FPGA.
- j) List the advantages R-2R type D/A converter.

SECTION-B

2. Convert 10000.0001 binary number to decimal number, hexadecimal and octal.
3. Reduce $F(A,B,C,D) = \sum m(1,3,5,7,9,11,13,15)$ to the simplest possible form using K-Map or Quine-McCluskey method.
4. Draw the logic diagram and explain the working of a successive approximation type A/D converter.
5. Draw the logic diagram and explain the working of a Master Slave JK flip-flop. What are its limitations? Also, mention how the limitation(s) of JK flip-flop are taken care in it.
6. Compare RAMs and ROMs. Also, discuss (in detail) the write operation in RAM.

SECTION-C

7. **Differentiate between:**
 - a) Ring and twisted ring counters.
 - b) Analog and digital systems.
 - c) Excess -3 and Gray codes.
 - d) Simplification by K-Map and Boolean-algebra.
8. Design a synchronous counter using JK flip flops that has the following sequence: 0000, 0010, 0101, 0110 and repeat. The undesired states must always go to 0000 on the next clock pulse.
9. **Discuss the following:**
 - a) Programmable array logic
 - b) Implementation of basic gates using NAND and NOR gates.

NOTE: Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.